UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/008,586	11/05/2001	Russell Francis	00CT18153314	2454

27975 7590 08/06/2004	EXAMINER	
ALLEN, DYER, DOPPELT, MILBRATH & GILCHRIST P.A. 1401 CITRUS CENTER 255 SOUTH ORANGE AVENUE P.O. BOX 3791 ORLANDO, FL 32802-3791	CHEN, TSE W	
	ART UNIT	PAPER NUMBER
	2116	

DATE MAILED: 08/06/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed
  after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any
  earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on _05 November 2001_.
2a) ☐ This action is **FINAL**.   2b) ☒ This action is non-final.
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is
   closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) _1-37_ is/are pending in the application.
   4a) Of the above claim(s) _1-11_ is/are withdrawn from consideration.
5) ☐ Claim(s) _____ is/are allowed.
6) ☒ Claim(s) _12-37_ is/are rejected.
7) ☐ Claim(s) _____ is/are objected to.
8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.
10) ☒ The drawing(s) filed on _13 February 2002_ is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
    a) ☒ All   b) ☐ Some * c) ☐ None of:
    1. ☒ Certified copies of the priority documents have been received.
    2. ☐ Certified copies of the priority documents have been received in Application No. _____.
    3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage
       application from the International Bureau (PCT Rule 17.2(a)).
    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
   Paper No(s)/Mail Date _11/5/2001_.
4) ☐ Interview Summary (PTO-413)
   Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1.   The information disclosure statement (IDS) submitted on November 5, 2001, was filed

before the mailing date of the first Office Action. The submission is in compliance with the

provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being

considered by the examiner.

Claim Rejections - 35 USC § 102

2.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the

basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3.   Claims 12-16, 19-23, 31-35 are rejected under 35 U.S.C. 102(b) as being anticipated by

Smith, U.S. Patent 5677849.

4.   In re claim 12, Smith discloses a system-on-chip (SOC) [integrated circuit] [col.1, ll.17-

23], comprising:

- A plurality of circuit blocks [fig.1; function blocks 11-14 with associated logic

  circuitries], each responsive to a respective local clock signal [clock signals 40-43] [col.2,

  ll.42-53; col.5, ll.65-66].

- At least one system clock [clk_in 35] connected to said circuit blocks for providing a

  system clock signal thereto for functioning as the respective local clock signals [col.3,

  l.63 -- col.4, l.34].

- A power control manager [central arbiter 1] connected to said circuit blocks for selectively providing a shutdown signal [start_clock 15-18] thereto [col.2, l.53 -- col.3, l.4; start_clock is set high to shut down].

- Each circuit block comprising a local power control circuit [NAND gates 27-30, 44-47, flip flops 23-26, inverters 36-39] for selectively maintaining the system clock signal as the local clock signal even after receiving the shutdown signal if the circuit block is in an active state when the shutdown signal is received [col.3, ll.5-12, ll.21-47; col.4, ll.35-53; kill_clock is low when circuit block is active].

5.   As to claims 13 and 21, Smith discloses that each local power control circuit comprises a clock separation circuit [NAND 44-47] connected to the power control manager for preventing the system clock signal from functioning as the respective local clock signal if said corresponding circuit block receiving the shutdown signal is in an idle state [fig.1; col.3, ll.5-12; high kill_clock is idle].

6.   As to claims 14 and 22, Smith discloses that the power control manager is connected to each local power control circuit through a respective clock enable line [start_clock lines 15-18] for providing the shutdown signal thereto [fig.1; col.3, ll.5-12].

7.   As to claim 15, Smith discloses that each circuit block further comprises a block logic circuit [inherently, some block logic circuit in the broadest interpretation is needed to perform a function] having a status line [kill_clock lines 19-22] connected to said local power control circuit for providing a status signal thereto indicating whether said circuit block is in the active or idle state [fig.1; col.3, ll.5-12; col.4, ll.35-53].

8.   As to claims 16 and 23, Smith discloses the local power control circuit that comprises a

logic circuit [NAND 44-47, flip flops 23-26, inverters 36-39] having a first input [NAND 44-47]

connected to the respective power down request line, a second input [NAND-44-47] connected

to the respective status line, and a third input [flip flops 23-26] connected to the system clock,

and an output for providing the local clock signal based upon logic states of the shutdown signal,

the status signal and the system clock signal [fig.1; col.3, ll.21-57; col.3, l.61 -- col.4, l.53].

9.   As to claim 19, Smith discloses said at least one system clock that comprises a plurality

of system clocks, each system clock for providing the system clock signal to selected circuit

blocks [fig.1; clk_in 35 is branched off to multiple system clocks to inputs 31-34 and 27-30 of

each block].

10.   In re claim 20, Smith discloses a system-on-chip (SOC) [integrated circuit] [col.1, ll.17-

23], comprising:

- A plurality of circuit blocks [fig.1; function blocks 11-14 with associated logic

  circuitries].

- A system clock [clk_in 35] connected to said circuit blocks for providing a system clock

  signal thereto [col.3, l.63 -- col.4, l.34].

- A power control manager [central arbiter 1] connected to said circuit blocks for

  selectively providing a shutdown signal [start_clock 15-18] thereto [col.2, l.53 -- col.3,

  l.4; start_clock is set high to shut down].

- Each circuit block comprising

- A block logic circuit [inherently, some block logic circuit in the broadest interpretation is needed in order to provide the status signal] providing a status signal [kill_clock] indicating whether said circuit block is in an active or idle state [col.3, ll.21-47].

- A local power control circuit [NAND gates 27-30, 44-47, flip flops 23-26, inverters 36-39] for selectively maintaining the system clock signal as a local clock signal even after receiving the shutdown signal if the status signal indicates said circuit block is in the active state when the shutdown signal is received [col.3, ll.5-12, ll.21-47; col.4, ll.35-53; kill_clock is low when circuit block is active].

11.   In re claims 31-35, Smith teaches the SOC as discussed above in reference to claims 12-16. Therefore, Smith teaches the method of operating the SOC.

Claim Rejections - 35 USC § 103

12.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13.   Claims 17-18, 24-25, 36-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Smith as applied to claims 14 and 22 above, and further in view of Matoba, U.S. Patent 5913068.

14.   In re claims 17-18 and 24-25, Smith discloses each and every limitation of the claim as discussed above in reference to claims 14 and 22. Smith did not discuss details of a register.

15.   Matoba discloses a system comprising:

- As to claims 17 and 24, a power control manager [system controller 15] that comprises at
  least one register [16a] connected to respective clock enable lines [intr 0-3] for storing
  data indicating logic states of the shutdown signals [col.8, ll.3-11, ll.48-53].

- As to claims 18 and 25, a central processing unit [CPU #0] connected to the power
  control manager [fig.1] for determining whether each circuit block [CPUs] is in the active
  or idle state by querying the at least one register [col.8, ll.3-11].

16.   It would have been obvious to one of ordinary skill in the art, having the teachings of

Smith and Matoba before him at the time the invention was made, to modify the SOC taught by

Smith to include the register and CPU taught by Matoba, in order to obtain the SOC of claims 17

and 18, comprising a power control manager comprising at least one register for storing data

indicating logic states of the shutdown signals and a central processing unit connected to said

power control manager for determining whether each circuit block is in an active state or an idle

state by querying said at least one register. One of ordinary skill in the art would have been

motivated to make such a combination as it provides a way for controlling power consumption

amongst multiple functional blocks through various detecting means [Matoba: col.1, l.60 -- col.2,

l.52].

17.   As to claims 36-37, Smith and Matoba teach the SOC as discussed above in reference to

claims 17-18. Therefore, Smith and Matoba teach the method of operating the SOC.

18.   Claims 26-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Smith in

view Matoba.

19.   In re claim 26, Smith discloses a system-on-chip (SOC) [integrated circuit] [col.1, ll.17-

23], comprising:

- A plurality of circuit blocks [fig.1; function blocks 11-14 with associated logic circuitries].

- A system clock [clk_in 35] connected to said circuit blocks for providing a system clock signal thereto [col.3, l.63 -- col.4, l.34].

- A power control manager [central arbiter 1] connected to said circuit blocks through a respective clock enable line [start_clock to NAND 44-47 which are part of respective circuit blocks] for selectively providing a shutdown signal [start_clock 15-18] thereto [col.2, l.53 -- col.3, l.4; start_clock is set high to shut down].

- Each circuit block comprising a local power control circuit [NAND gates 27-30, 44-47, flip flops 23-26, inverters 36-39] for selectively maintaining the system clock signal as a local clock signal even after receiving the shutdown signal if the the circuit block is in the active state when the shutdown signal is received [col.3, ll.5-12, ll.21-47; col.4, ll.35-53; kill_clock is low when circuit block is active].

20.   Smith did not discuss details of a register.

21.   Matoba discloses a system comprising:

- A power control manager [system controller 15] that comprises at least one register [16a] connected to clock enable lines [intr 0-3] for storing data indicating logic states of the shutdown signals [col.8, ll.3-11, ll.48-53].

- A central processing unit [CPU #0] connected to the power control manager [fig.1] for determining whether each circuit block [CPUs] is in the active or idle state by querying the at least one register [col.8, ll.3-11].

22.   It would have been obvious to one of ordinary skill in the art, having the teachings of

Smith and Matoba before him at the time the invention was made, to modify the SOC taught by

Smith to include the register and CPU taught by Matoba, in order to obtain the SOC of claims 17

and 18, comprising a power control manager comprising at least one register for storing data

indicating logic states of the shutdown signals and a central processing unit connected to said

power control manager for determining whether each circuit block is in an active state or an idle

state by querying said at least one register. One of ordinary skill in the art would have been

motivated to make such a combination as it provides a way for controlling power consumption

amongst multiple functional blocks through various detecting means [Matoba: col.1, 1.60 -- col.2,

l.52].

23.   As to claim 27, Smith discloses that each local power control circuit comprises a clock

separation circuit [NAND 44-47] connected to the power control manager for preventing the

system clock signal from functioning as the local clock signal if said corresponding circuit block

receiving the shutdown signal is in an idle state [fig.1; col.3, ll.5-12; high kill_clock is idle].

24.   As to claim 28, Smith discloses that the power control manager is connected to each local

power control circuit through a respective clock enable line [start_clock lines 15-18] for

providing the shutdown signal thereto [fig.1; col.3, ll.5-12].

25.   As to claim 29, Smith discloses that each circuit block further comprises a block logic

circuit [inherently, some block logic circuit in the broadest interpretation is needed to perform a

function] having a status line [kill_clock lines 19-22] connected to said local power control

circuit for providing a status signal thereto indicating whether said circuit block is in the active or

idle state [fig.1; col.3, ll.5-12; col.4, ll.35-53].

26.   As to claim 30, Smith discloses the local power control circuit that comprises a logic

circuit [NAND 44-47, flip flops 23-26, inverters 36-39] having a first input [NAND 44-47]

connected to the respective power down request line, a second input [NAND-44-47] connected

to the respective status line, and a third input [flip flops 23-26] connected to the system clock,

and an output for providing the local clock signal based upon logic states of the shutdown signal,

the status signal and the system clock signal [fig.1; col.3, ll.21-57; col.3, l.61 -- col.4, l.53].

Conclusion

27.   The prior art made of record and not relied upon is considered pertinent to applicant's

disclosure.

a.   Jung et al., U.S. Patent 5768213, discloses a clock control circuit for multiple

function blocks.

b.   Ohta, U.S. Patent 6342795, discloses a clock control circuit with an input

indicating the active or idle state of the function block.

c.   Jain et al., U.S. Patent 6633987, discloses a clock control system with multiple

function blocks.

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Tse Chen whose telephone number is (703) 305-8580. The

examiner can normally be reached on Monday - Friday 9AM - 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Lynne Browne can be reached on (703) 308-1159. The fax phone number for the

organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent

Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR

system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tse Chen
August 2, 2004

REHANA PERVEEN
PRIMARY EXAMINER